19-0695; Rev 0; 1/07

Dual Comparator/Terminator with Cable-Droop Compensation

General Description

The MAX9955 high-speed, dual comparator/terminator IC includes a dual comparator and a terminator for each channel. The dual comparator features programmable cable-droop compensation at its input and offers low dispersion (timing variation) over a wide variety of input conditions, programmable hysteresis, and differential outputs. The terminator provides a 50Ω buffered termination to a programmed level. The MAX9955 comparator operating range is -1.1V to +3.6V, and the terminator operating range is -1.0V to +3.5V.

The MAX9955 comparator provides high-speed, open-collector outputs with internal 50Ω termination resistors that are compatible with doubly terminated 0.4V_{P-P} (typ) CML. These features significantly reduce the discrete component count on the circuit board.

The MAX9955 power dissipation is only 800mW per channel under static conditions and 850mW per channel at 2Gbps toggling conditions. The device is available in a 64-pin, 10mm x 10mm body and 0.5mm pitch TQFP. A 5mm x 5mm exposed die paddle on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +50°C to +90°C, and features a die temperature monitor output.

Applications

High-Performance Memory Automated Test Equipment (DDR3, GDDR3, GDDR4)

High-Performance SOC Automated Test Equipment

Selector Guide and Typical Operating Circuit located at end of data sheet.

Features

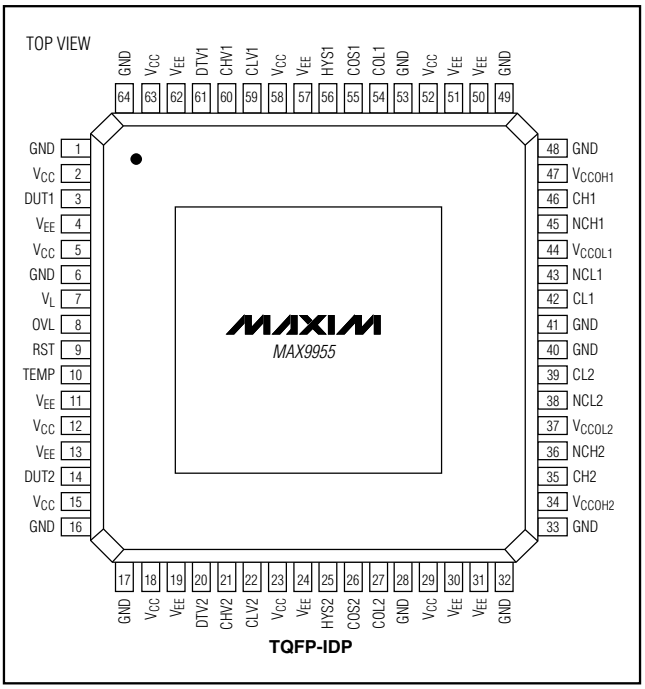
- **Cable-Droop Compensation**
- **55ps Input Equivalent Rise/Fall Time**
- **190ps Minimum Pulse Width**
- **Low Power Dissipation**
  850mW per Channel at 2Gbps (typ)
- **Low Timing Dispersion**
- **Integrated Terminator**
- **Comparator Hysteresis Control from 0 to 10mV**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9955BDCCB	0°C to +70°C	64 TQFP-IDP*	C64E-4R

**IDP = Inverted die paddle (exposed paddle on top of device).*
Note: *Device is available in both leaded and lead-free packaging. Specify lead free by adding a + symbol at the end of part number when ordering.*

Pin Configuration



TQFP-IDP

Dual Comparator/Terminator with Cable-Droop Compensation

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +8V
V_{EE} to GND.....-6V to +0.3V
V_{CC} - V_{EE}.....-0.3V to +14V
V_L to GND.....-0.3V to +4.1V
DUT_ to GND.....-2V to +4.5V
CH_, NCH_, CL_, NCL_ to GND .....-0.3V to ($V_{CCO\_\_}$ + 2V)
$V_{CCO\_\_}$ to GND.....-0.3V to +4.1V
OVL to GND .....-0.3V to (V_L + 0.3V)
OVL Current.....±10mA
RST to GND .....-0.3V to +5V
DTV_, CHV_, CLV_ to GND .....-2V to +4.5V
CHV_ or CLV_ to DUT_.....±5V
COS_, COL_ to GND.....-0.3V to +4.1V
HYS_ Current.....±1mA
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TEMP Current.....-0.5mA to +20mA
DUT_ Current.....±80mA
DUT_ Short Circuit to -1.0V to +3.5V.....Continuous
Continuous Power Dissipation (T_A = +70°C)
MAX9955 (derate 125mW/°C above +70°C).....10W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+125°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage value is based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 7V, V_{EE} = -5V, V_L = 3.3V, $V_{CCO\_\_}$ = 3.3V, $V_{CHV\_}$ = $V_{CLV\_}$ = 0, $V_{DTV\_}$ = 0.5V, $V_{COS\_}$ = $V_{COL\_}$ = 0, HYS_ = unconnected, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		6.75	7.0	7.50	V
Negative Supply	V_{EE}		-5.50	-5.0	-4.75	V
Positive Supply Current	I_{CC}	R_L ≥ 10MΩ (Note 2)	102	112	121	mA
Negative Supply Current	I_{EE}	R_L ≥ 10MΩ (Note 2)	150	162	174	mA
Power Dissipation (Note 2)	P_D	R_L ≥ 10MΩ		1.6	1.8	W
		$V_{DUT\_}$ = 0 to 2V at 2Gbps, $V_{DTV\_}$ = 1V (Note 3)		1.7		
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 4)	-1.1		+3.5	V
Input Return Loss (Note 5)		1GHz		-24		dB
		2GHz		-20		
Input Return Loss by Time Domain Reflectometry		$V_{DUT\_}$ = 0 to 1V, t_R = t_F = 150ps (Note 6)		6.0		%
LEVEL PROGRAMMING INPUTS (DTV_, CHV_, CLV_, COS_, COL_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling Time		To 0.1% of full-scale change (Note 5)		1		µs
SINGLE-ENDED CONTROL INPUT (RST)						
Input High Voltage	V_{IH}		1.65		3.50	V
Input Low Voltage	V_{IL}		-0.10		+0.85	V
Input Bias Current	I_B				±25	µA
SINGLE-ENDED OUTPUT (OVL)						
Digital Supply	V_L		3.0	3.3	3.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 7V, V_{EE} = -5V, V_L = 3.3V, $V_{CCO\_\_}$ = 3.3V, $V_{CHV\_}$ = $V_{CLV\_}$ = 0, $V_{DTV\_}$ = 0.5V, $V_{COS\_}$ = $V_{COL\_}$ = 0, HYS_ = unconnected, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Current	I_L	R_{OVL} = open	0.5	1	2.0	mA
Output High Voltage			V_L - 0.4		V_L	V
Output Low Voltage			0		0.4	V
Rise and Fall Time		C_L = 20pF		3.6		ns
Overcurrent Detect Threshold			±50		±80	mA
TEMPERATURE MONITOR (TEMP)						
Nominal Voltage		T_J = +70°C, $R_L \geq 10M\Omega$ (Note 8)	3.30	3.52	3.75	V
Temperature Coefficient				+10		mV/°C
Output Resistance		I_{TEMP} = 0µA, 10µA	18	24	30	kΩ
COMPARATORS (Note 9)						
DC CHARACTERISTICS						
Input Voltage Range	V_{IN}		-1.1		+3.6	V
Differential Input Voltage	V_{DIFF}		±4.7			V
Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V, COS = 0V, COL = 0V			±20	mV
		$V_{DUT\_}$ = 1.5V, COS = 3.3V, COL = 3.3V			±20	
Offset-Voltage Temperature Coefficient				±50		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = -1.1V, +3.6V (Note 10)		±0.3	±3.0	mV/V
Linearity Error		$V_{DUT\_}$ = -1.1V, +1V, +3.6V (Note 11)			±15	mV
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V (Note 12)		±0.3	±3.0	mV/V
Gain				360		V/V
HYSTERESIS						
Hysteresis Range		R_{HYS} = open, 2kΩ (Note 13)	0		10	mV
Input Hysteresis		R_{HYS} = open		1.0		mV
		R_{HYS} = 3.3kΩ		2.5		
		R_{HYS} = 2.7kΩ		6.5		
		R_{HYS} = 2.4kΩ		9.5		
Hysteresis Setting Accuracy		R_{HYS} = 3.0kΩ (5mV setting)		±2		mV
AC CHARACTERISTICS (Note 14)						
Input Equivalent Rise and Fall Time		$t_R = t_F$ = 60ps, 20% to 80% (Note 7)		55	90	ps
Minimum Pulse Width	$t_{PW(MIN)}$	$t_R = t_F$ = 80ps, (Notes 7, 15)		190	250	ps
Prop Delay	t_{PDL}	(Note 7)	0.35	0.5	0.65	ns
Prop-Delay Temperature Coefficient				+0.5		ps/°C
Prop Delay Match, High/Low vs. Low/High		(Note 7)		±5	±20	ps
Prop Delay Match, Comparators within Package		(Note 16)		±5		ps

Dual Comparator/Terminator with Cable-Droop Compensation

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 7V, V_{EE} = -5V, V_L = 3.3V, $V_{CCO\_\_}$ = 3.3V, $V_{CHV\_}$ = $V_{CLV\_}$ = 0, $V_{DTV\_}$ = 0.5V, $V_{COS\_}$ = $V_{COL\_}$ = 0, HYS_ = unconnected, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop Delay Dispersion vs. Common Mode (Notes 7, 17)		$V_{CHV\_}$ = $V_{CLV\_}$ = 0 to 2V, relative to 0.5V		±2	±10	ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.1V to +3.6V, relative to 0.5V		±15	±25	
Waveform Tracking, 10% to 90%		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 150ps, 10% to 90% relative to timing at 50% point (Note 7)		±10	±35	ps
Prop Delay Dispersion vs. Pulse Width (Note 7)		$V_{DUT\_}$ = $1V_{P-P}$, 0.5ns to 24.5ns pulse width, relative to 12.5ns pulse width, t_R = t_F = 80ps		±10	±20	ps
		$V_{DUT\_}$ = $1V_{P-P}$, 0.2ns to 24.8ns pulse width, relative to 12.5ns pulse width, t_R = t_F = 80ps		±15	±25	
Prop Delay Dispersion vs. Slew Rate		$V_{DUT\_}$ = $1V_{P-P}$, 2V/ns to 6V/ns slew rate, relative to 4V/ns slew rate (Note 7)		±15	±35	ps
Peaking		$V_{COS\_}$ = $V_{COL\_}$ = 0		0		%
		$V_{COS\_}$ = 0, $V_{COL\_}$ = 3.3V		20		
		$V_{COS\_}$ = 3.3V, $V_{COL\_}$ = 0		20		
		$V_{COS\_}$ = $V_{COL\_}$ = 3.3V (Note 7)	20	40		
Input Voltage Range COS_, COL_		(Note 7)	0		3.3	V
LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_)						
$V_{CCO\_\_}$ Voltage Range	$V_{VCCO\_\_}$		1.0		3.6	V
$V_{CCO\_\_}$ Current	$I_{VCCO\_\_}$			70		mA
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0	$V_{CCO\_\_}$ - 0.1	$V_{CCO\_\_}$ - 0.03	$V_{CCO\_\_}$ + 0.02	V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0		$V_{CCO\_\_}$ - 0.8		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0	750	800	850	mV
Internal Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_	48	50	52	Ω
Differential Rise and Fall Times	t_R, t_F	20% to 80%		90		ps
TERMINATOR						
DC CHARACTERISTICS (R_L ≥ 10MΩ)						
DTV_ Voltage Range	$V_{DTV\_}$	(Note 4)	-1.0		+3.5	V
Offset Voltage	V_{OS}	$V_{DTV\_}$ = 1.25V			±20	mV
Offset-Voltage Temperature Coefficient				±50		µV/°C
Gain	A_V	$V_{DTV\_}$ = 0 and 2V	0.997		1.003	V/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 7V, V_{EE} = -5V, V_L = 3.3V, $V_{CCO\_\_}$ = 3.3V, $V_{CHV\_}$ = $V_{CLV\_}$ = 0, $V_{DTV\_}$ = 0.5V, $V_{COS\_}$ = $V_{COL\_}$ = 0, HYS_ = unconnected, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Temperature Coefficient				-20		ppm/°C
Linearity Error		$V_{DTV\_}$ = -1V, +1V, +3.5V (Note 11)			±15	mV
Power-Supply Rejection Ratio	PSRR	$V_{DTV\_}$ = 1.5V (Note 12)			±18	mV/V
DC Output Resistance	$R_{DUT\_}$	$V_{DTV\_}$ = 1.25V, $I_{DUT\_}$ = 8mA, $\Delta I_{DUT\_}$ = ±2.5mA (Note 18)	48	50	52	Ω
DC Output Resistance Variation		$V_{DTV\_}$ = 1.25V, $I_{DUT\_}$ = ±1mA, ±8mA, $\Delta I_{DUT\_}$ = ±2.5mA		0.3	1	Ω
		$V_{DTV\_}$ = 1.25V, $I_{DUT\_}$ = ±1mA, ±8mA, ±15mA, ±40mA, $\Delta I_{DUT\_}$ = ±2.5mA		0.8	2	

Note 1: All minimum and maximum values are tested at nominal supply voltages and T_J = +70°C with an accuracy of ±15°C, unless otherwise noted. Rise and fall times are measured using 10% and 90% points, unless otherwise noted.
Note 2: Total for dual device.
Note 3: Does not include above ground internal dissipation of the comparator outputs. Additional power dissipation is typically (64mA x $V_{VCCO\_\_}$).
Note 4: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.
Note 5: Based on simulation results only.
Note 6: Output return loss by time domain reflectometry (%) = 100 x (reflection amplitude / drive amplitude). See Figure 1.

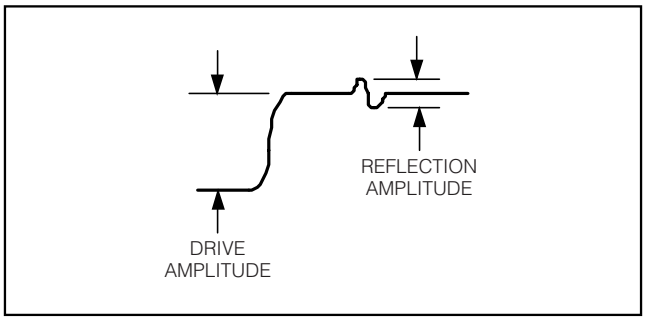


Figure 1. TDR Return Loss

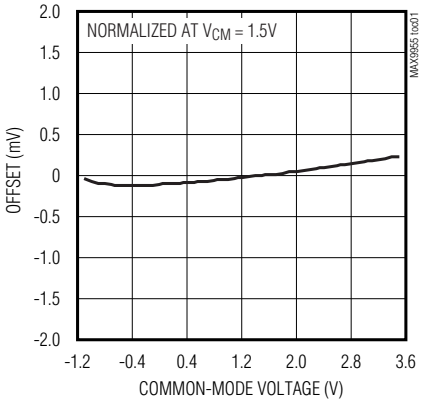
Note 7: Guaranteed by design and characterization. Not production tested.
Note 8: Verified at wafer sort.
Note 9: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
Note 10: Change in offset voltage over the input range.
Note 11: Relative to straight line between 0 and 2V.
Note 12: Change in offset voltage with power supplies independently set to their minimum and maximum values.
Note 13: Minimum specification not tested. Under the condition R_{HYS} = open, the circuit is designed to have no hysteresis.
Note 14: Unless otherwise noted, all comparator AC characteristics are measured at 40MHz, $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 150ps, Z_S = 50Ω, $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to 1.25V and $V_{CCO\_}$ = 2.5V. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.
Note 15: At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.
Note 16: Rising edge to rising edge or falling edge to falling edge.
Note 17: $V_{DUT\_}$ = $1V_{P-P}$. Overdrive = 500mV.
Note 18: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Dual Comparator/Terminator with Cable-Droop Compensation

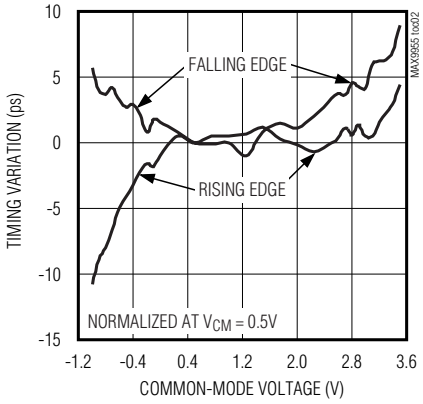
Typical Operating Characteristics

(T_J = +70°C, unless otherwise noted.)

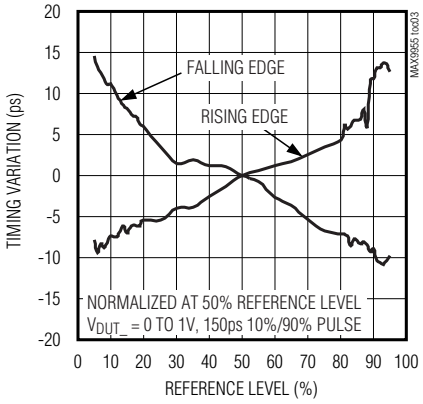
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



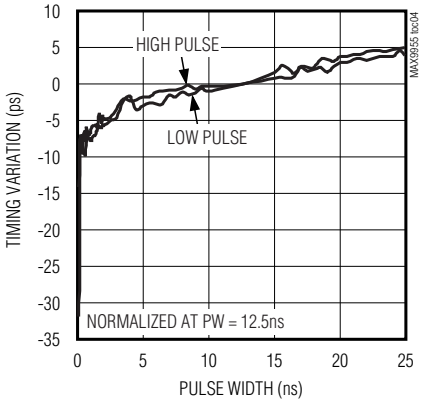
COMPARATOR TIMING VARIATION vs. COMMON-MODE VOLTAGE



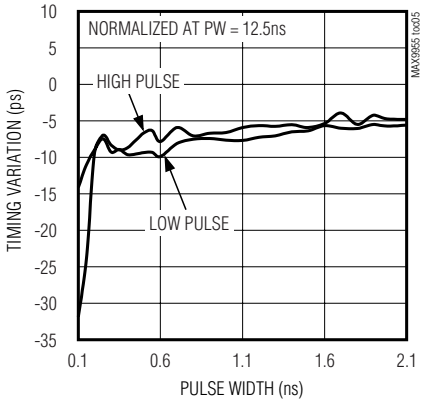
COMPARATOR WAVEFORM TRACKING



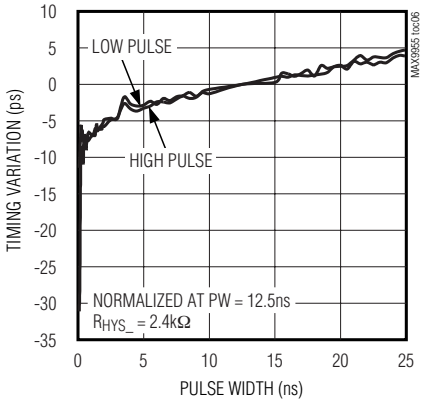
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



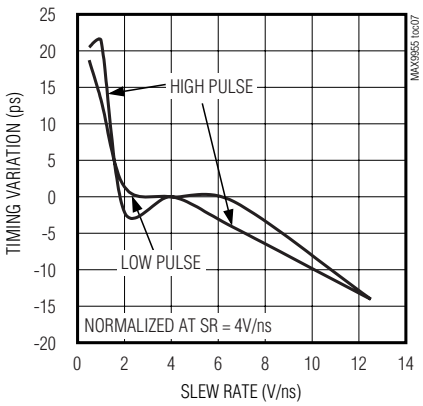
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



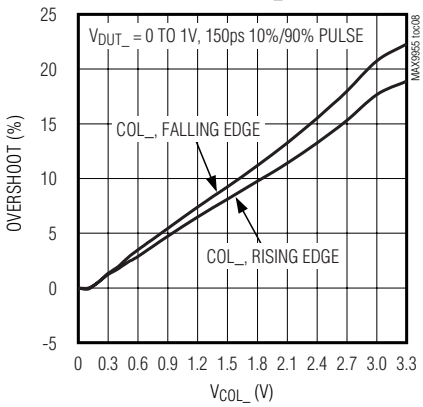
COMPARATOR WITH HYSTERESIS TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



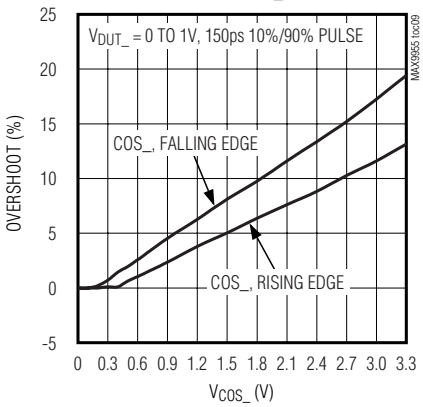
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



COMPARATOR PEAKING vs. $V_{COL\_}$



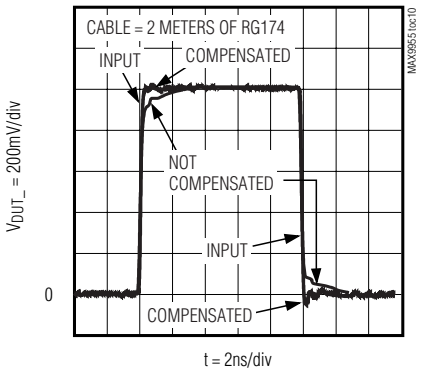
COMPARATOR PEAKING vs. $V_{COS\_}$



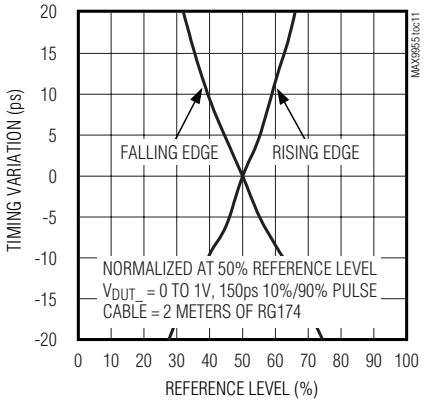
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

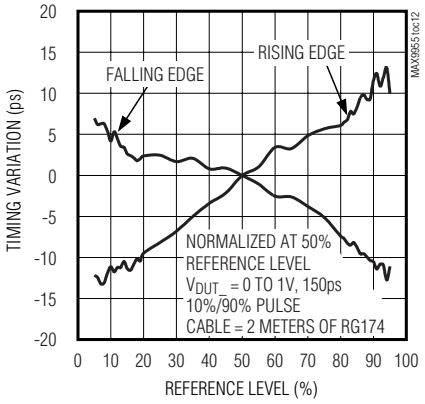
COMPARATOR REDIGITIZATION WITH CABLE COMPENSATION, RISING EDGE



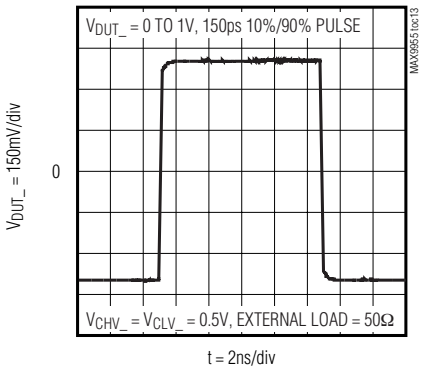
COMPARATOR WAVEFORM TRACKING WITHOUT CABLE COMPENSATION



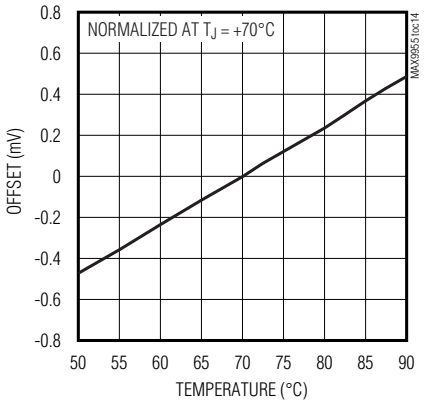
COMPARATOR WAVEFORM TRACKING WITH CABLE COMPENSATION



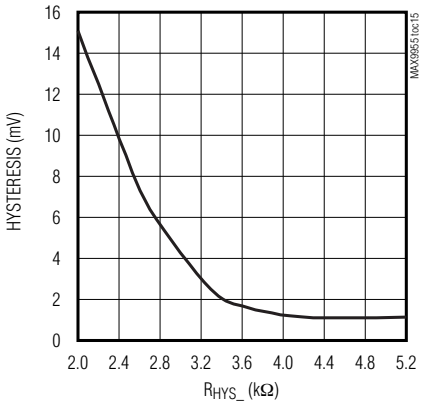
COMPARATOR DIFFERENTIAL OUTPUT RESPONSE



COMPARATOR OFFSET vs. TEMPERATURE



COMPARATOR HYSTERESIS vs. $R_{HYS\_}$ TO GND

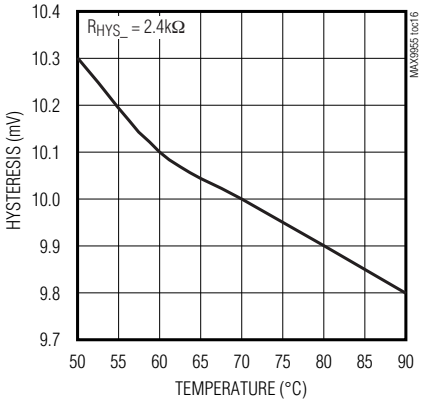


Dual Comparator/Terminator with Cable-Droop Compensation

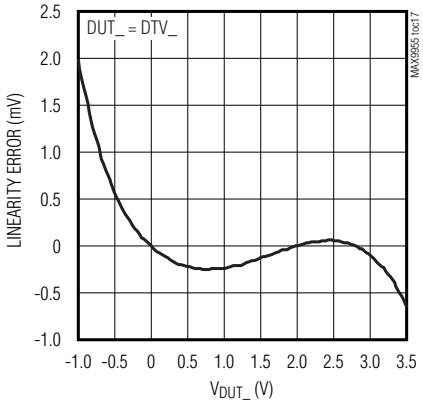
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

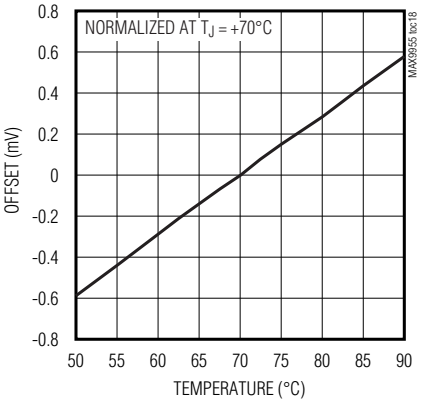
COMPARATOR HYSTERESIS vs. TEMPERATURE



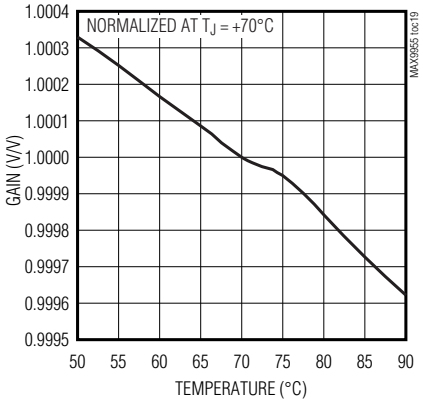
TERMINATOR LINEARITY ERROR vs. OUTPUT VOLTAGE



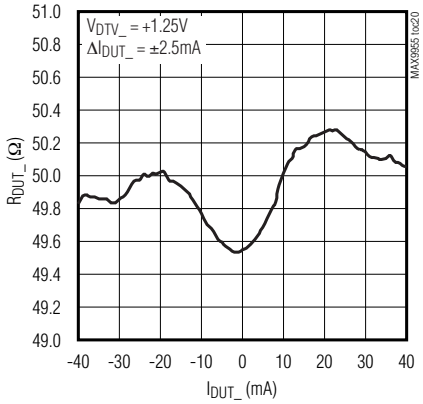
TERMINATOR OFFSET vs. TEMPERATURE



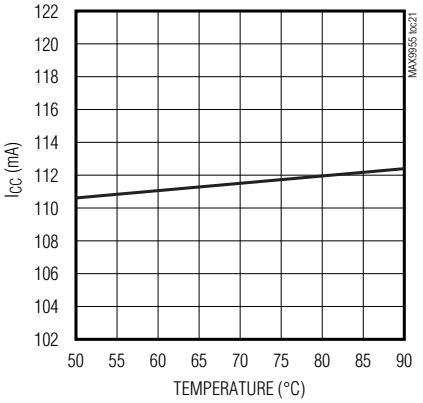
TERMINATOR GAIN vs. TEMPERATURE



TERMINATOR OUTPUT RESISTANCE vs. $I_{DUT\_}$



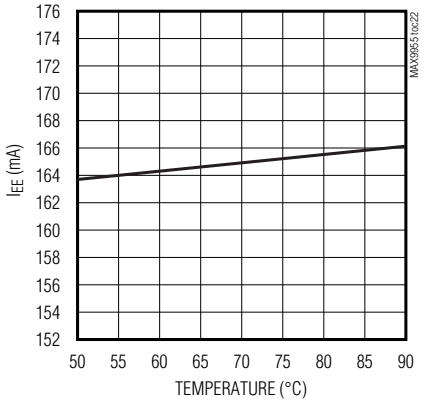
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



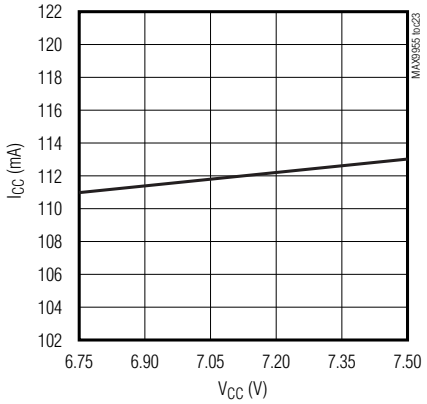
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

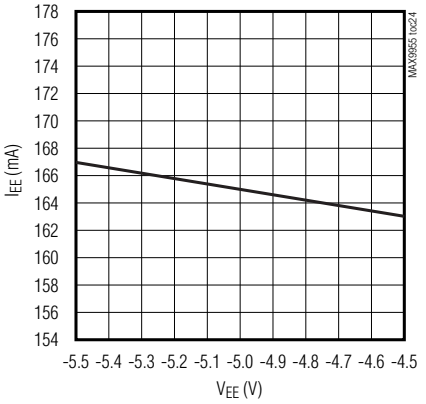
NEGATIVE SUPPLY CURRENT vs. TEMPERATURE



POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE



NEGATIVE SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 6, 16, 17, 28, 32, 33, 40, 41, 48, 49, 53, 64	GND	Ground Connection
2, 5, 12, 15, 18, 23, 29, 52, 58, 63	V_{CC}	Positive Power-Supply Input
3	DUT1	Channel 1 Device-Under-Test Input. Combined input for comparator and terminator.
4, 11, 13, 19, 24, 30, 31, 50, 51, 57, 62	V_{EE}	Negative Power-Supply Input
7	V_L	Logic Power-Supply Input. Sets the V_{OH} level for OVL.
8	OVL	Overcurrent Flag Output. OVL goes high when the terminator buffer of channel 1 or 2 exceeds the current limit.
9	RST	Reset Input. Resets the OVL flag to low and closes the buffer output switch.
10	TEMP	Temperature Monitor Output
14	DUT2	Channel 2 Device-Under-Test Input. Combined input for comparator and terminator.
20	DTV2	Channel 2 Terminator Reference Input
21	CHV2	Channel 2 High Comparator Reference Input
22	CLV2	Channel 2 Low Comparator Reference Input
25	HYS2	Channel 2 Hysteresis Input
26	COS2	Channel 2 Short-Duration Cable-Droop Compensation Input

Dual Comparator/Terminator with Cable-Droop Compensation

Pin Description (continued)

PIN	NAME	FUNCTION
27	COL2	Channel 2 Long-Duration Cable-Droop Compensation Input
34	V_{CCOH2}	Channel 2 High Comparator Collector Voltage Input. Voltage input for channel 2 high comparator output termination resistors. Provides pullup voltage and current for the output termination resistors.
35	CH2	Channel 2 High Comparator Positive Output
36	NCH2	Channel 2 High Comparator Negative Output
37	V_{CCOL2}	Channel 2 Low Comparator Collector Voltage Input. Voltage input for channel 2 low comparator output termination resistors. Provides pullup voltage and current for the output termination resistors.
38	NCL2	Channel 2 Low Comparator Negative Output
39	CL2	Channel 2 Low Comparator Positive Output
42	CL1	Channel 1 Low Comparator Positive Output
43	NCL1	Channel 1 Low Comparator Negative Output
44	V_{CCOL1}	Channel 1 Low Comparator Collector Voltage Input. Voltage input for channel 1 low comparator output termination resistors. Provides pullup voltage and current for the output termination resistors.
45	NCH1	Channel 1 High Comparator Negative Output
46	CH1	Channel 1 High Comparator Positive Output
47	V_{CCOH1}	Channel 1 High Comparator Collector Voltage Input. Voltage input for channel 1 high comparator output termination resistors. Provides pullup voltage and current for the output termination resistors.
54	COL1	Channel 1 Long-Duration Cable-Droop Compensation Input
55	COS1	Channel 1 Short-Duration Cable-Droop Compensation Input
56	HYS1	Channel 1 Hysteresis Input
59	CLV1	Channel 1 Low Comparator Reference Input
60	CHV1	Channel 1 High Comparator Reference Input
61	DTV1	Channel 1 Terminator Reference Input
—	EP	Exposed Paddle. Exposed paddle is used for heat removal. EP is internally connected to V_{EE}. Connect EP to V_{EE} or leave unconnected.

Detailed Description

The MAX9955 high-speed, dual comparator/terminator IC includes a dual comparator and a terminator for each channel. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, programmable cable-droop compensation, programmable hysteresis, and differential outputs. The terminator provides a 50Ω buffered termination to a programmed level. The MAX9955 comparator operating range is -1.1V to +3.6V, and the terminator operating range is -1.0V to +3.5V.

The MAX9955 comparator provides high-speed open-collector outputs with internal 50Ω termination resistors that are compatible with doubly terminated 0.4V_{P-P} (typ) CML. These features significantly reduce the discrete component count on the circuit board and improve circuit performance. Figure 2 shows a functional diagram of the MAX9955.

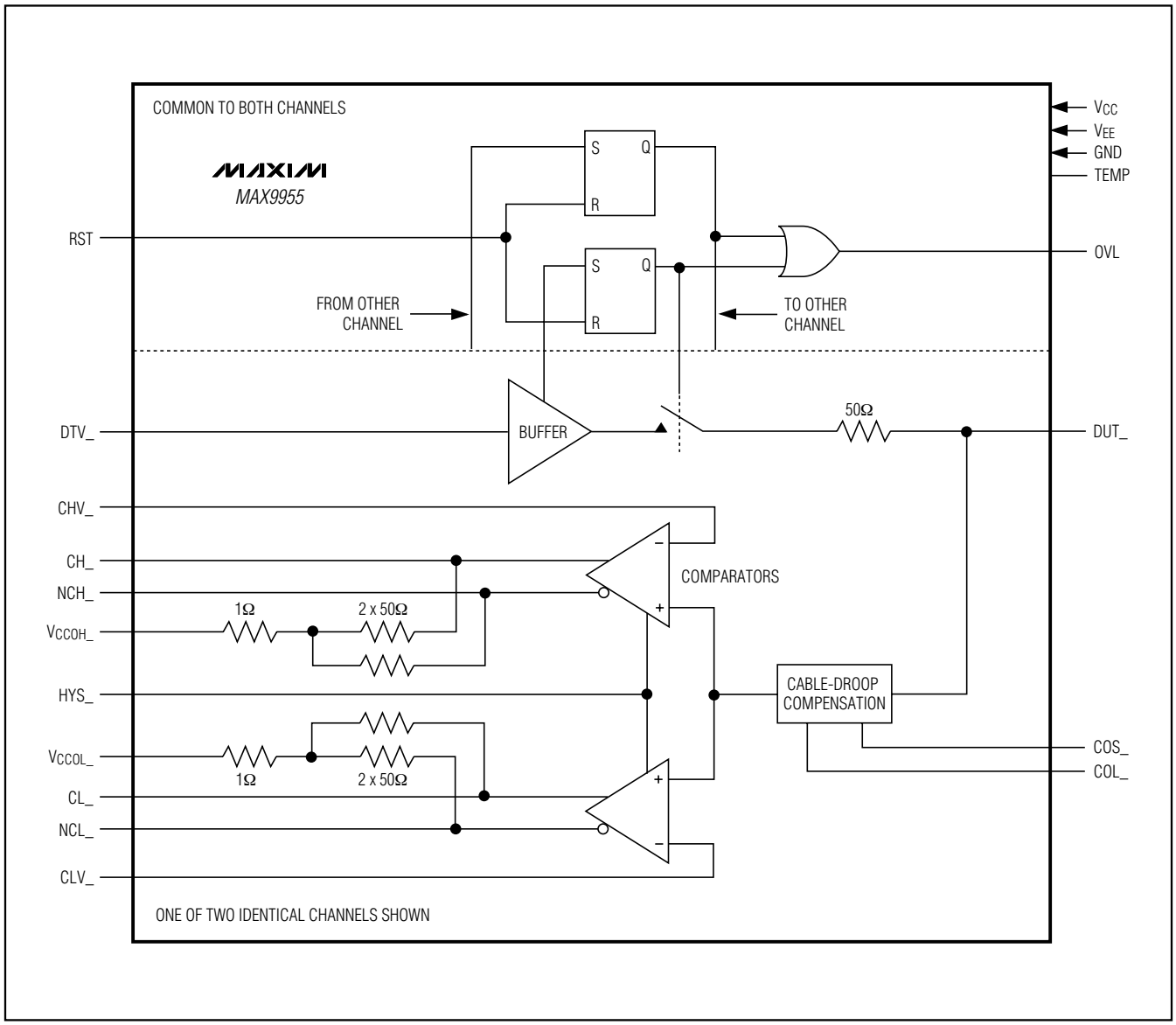


Figure 2. Functional Diagram

Dual Comparator/Terminator with Cable-Droop Compensation

Buffer Termination and OVL

The MAX9955 provides a 50Ω series termination to the DTV_ buffer output. The nominal terminator resistance is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Buffer output current is monitored and limited to ±50mA (min). The buffer output switch opens and OVL latches high when the output current exceeds ±50mA. Asserting RST closes the buffer output switch and resets OVL. The single RST input controls both channels.

Comparators

The MAX9955 provides two independent high-speed comparators for each channel. Each comparator provides one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see Figure 2). Comparator outputs are a logical result of the input conditions, as indicated in Table 1. The comparator differential outputs are open collector to ease interfacing with a wide variety of logic families. Internal termination resistors switch a 16mA current source between the two outputs (Figure 3). The termination resistors connect the outputs to voltage termination inputs $V_{CCOH\_}$ and $V_{CCOL\_}$. Connect the termination inputs to the desired V_{OH} voltage. Each output provides a nominal 800mV$_{P-P}$ swing and 50Ω source termination. If an additional external 50Ω destination termination is used to double-terminate the line, the nominal 800mV swing is halved.

Table 1. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CL_, NCL_	CH_, NCH_
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

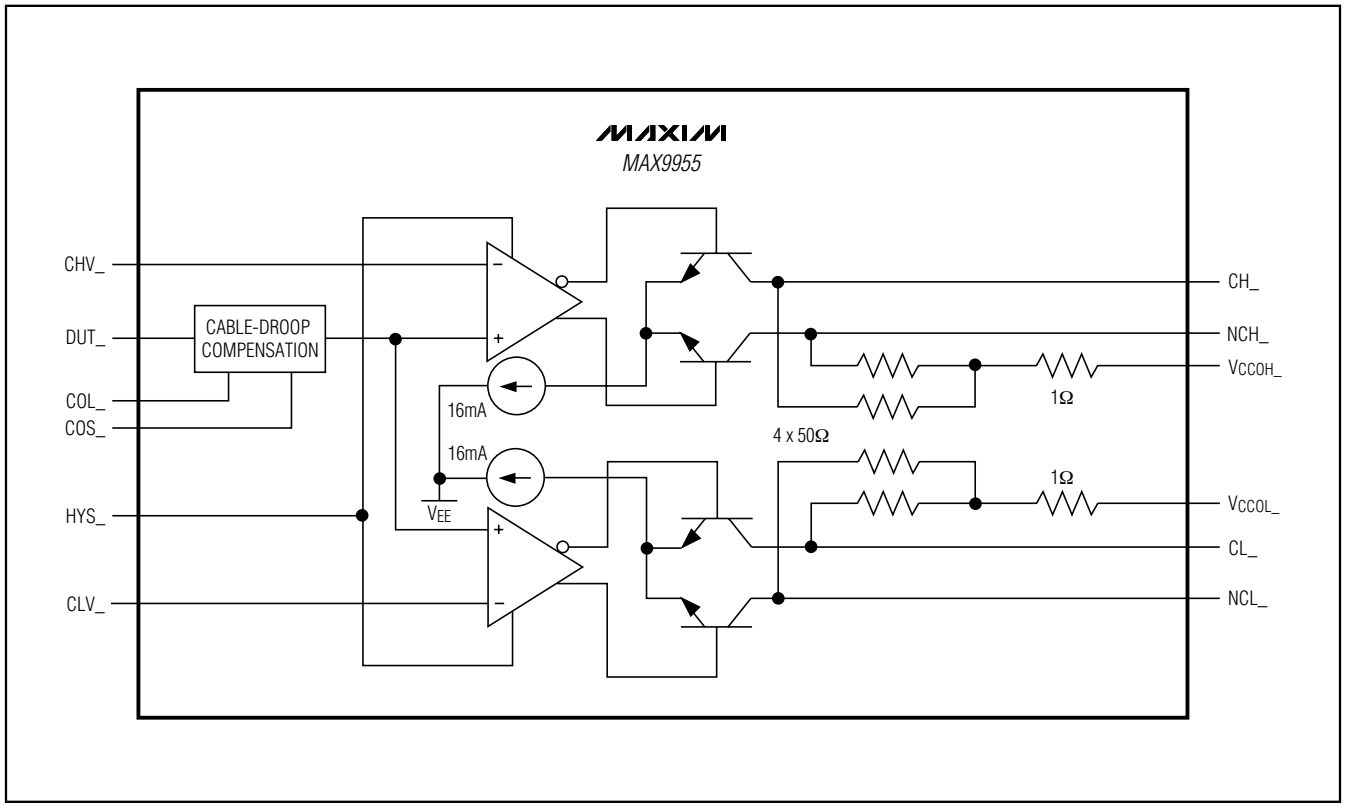


Figure 3. Comparator Functional Diagram

Cable-Droop Compensation

The comparator inputs incorporate cable-droop compensation. At high frequencies, cable loss degrades the comparator input waveform at DUT_. The cable-droop circuit compensates this loss by adding two peaking single time-constant decaying waveforms to the DUT_ waveform. In the frequency domain, the DUT_ function is multiplied by two zero-pole pairs (see Figure 4). Analog voltage inputs COS_ and COL_ control the peaking amplitude. The time constants are fixed. COS_ varies the amplitude of the high-frequency boost; its time constant is 50ps (typ). COL_ varies the amplitude of the low-frequency boost; its time constant is 1.5ns (typ). See the *Typical Operating Characteristics* for peaking versus COS_ and COL_ voltages. Connect COS_ and COL_ to GND if compensation is not required.

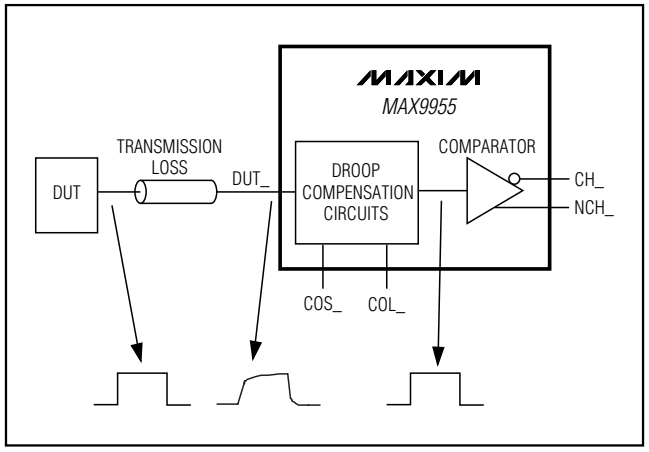


Figure 4. Cable-Droop Compensation

Hysteresis

The comparator function incorporates hysteresis. Hysteresis rejects noise and prevents oscillations on low-slew-rate input signals. External resistors control hysteresis levels. With HYS_ unconnected, the programmed hysteresis is 0mV (min). Connect an external resistor between HYS_ and GND to program nonzero hysteresis. See the *Typical Operating Characteristics* for resistance values.

Temperature Monitor

The MAX9955 supplies a temperature output signal, TEMP, that asserts a 3.52V nominal output voltage at +70°C (343K) die temperature. The output voltage changes proportionally with temperature at 10mV/°C.

Power-Supply Considerations

Bypass power supply pins V_{CC} and V_{EE} with 0.01µF capacitors to GND at the device, and use bulk bypassing of at least 10µF on each supply. Bypass $V_{CCO\_}$ _ and V_L with 0.01µF at the device.

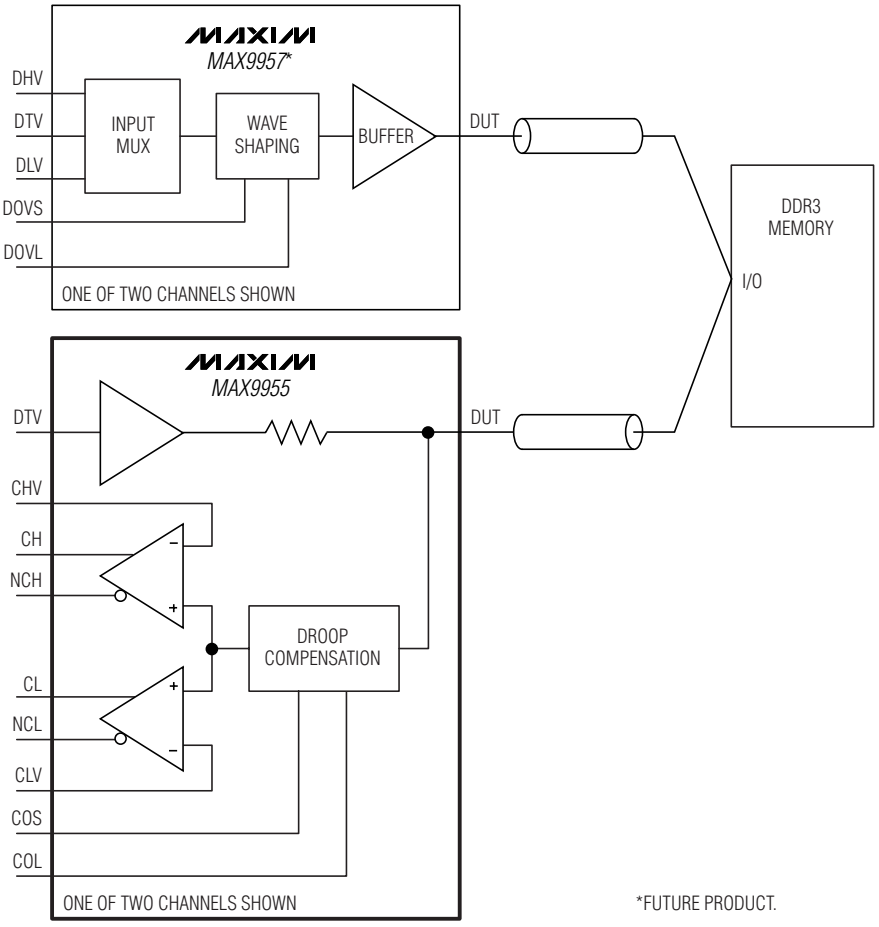
Chip Information

TRANSISTOR COUNT: 2297

PROCESS: Bipolar

Dual Comparator/Terminator with Cable-Droop Compensation

Typical Operating Circuit



Selector Guide

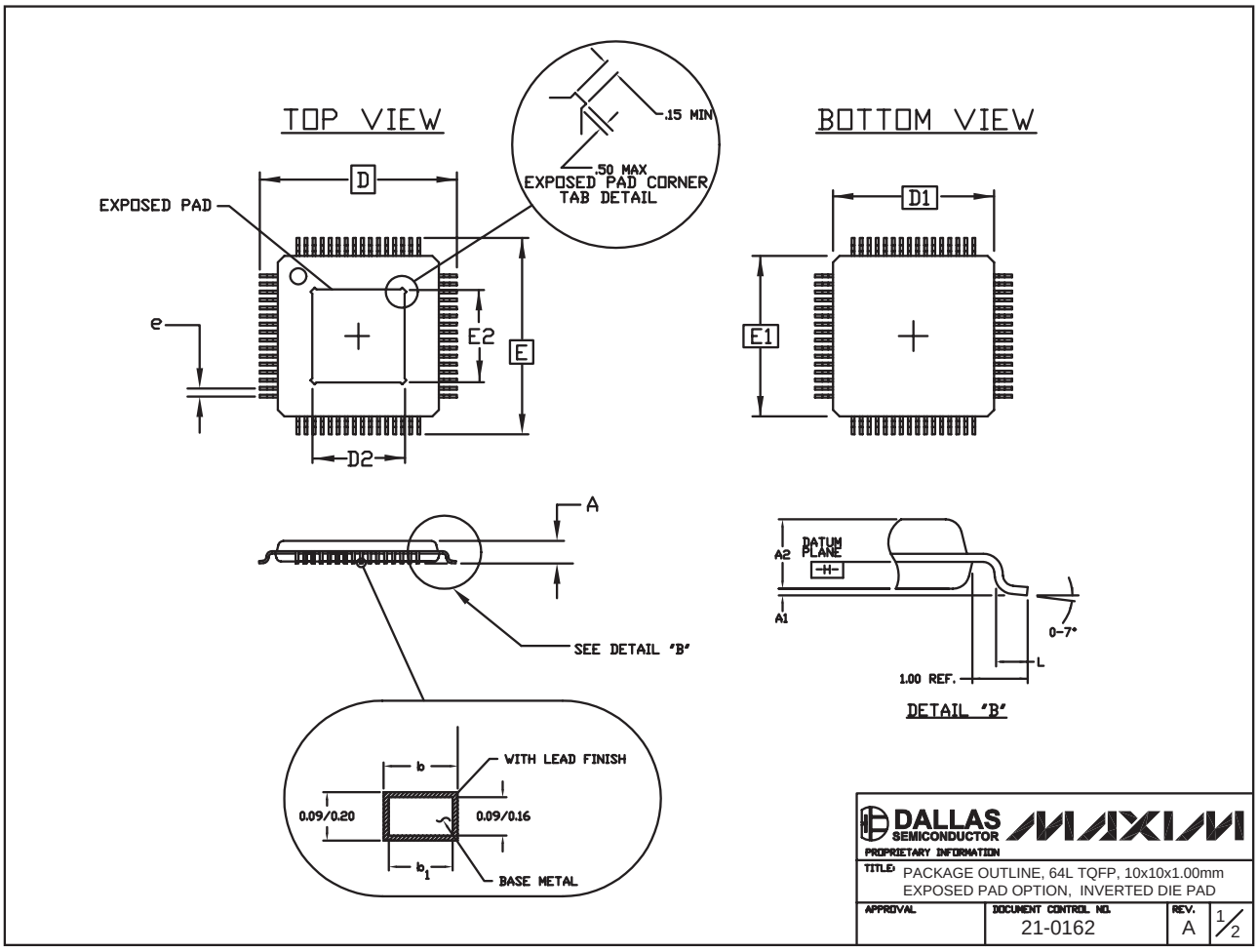
PART	RANGE	COMPARATOR OUTPUT TERMINATION	HEAT EXTRACTION
MAX9955BDCCB	-1.1V to +3.6V	50Ω to $V_{CCO\_\_}$	Top

Dual Comparator/Terminator with Cable-Droop Compensation

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

64L TQFP.EPS



Dual Comparator/Terminator with Cable-Droop Compensation

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY AS MUCH AS 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. MEET JEDEC MS-026 EXCEPT FOR COPLANARITY (SEE NOTE 8).
8. LEADS SHALL BE COPLANAR WITHIN 0.10 MM.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. REFER TO PRODUCT DATA SHEET FOR PACKAGE CODE.

SYMBOL	COMMON DIMENSIONS ALL DIMENSIONS IN MILLIMETERS	
	JEDEC VARIATION ACD	
	MIN.	MAX.
A		1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	12.00 BSC.	
D_1	10.00 BSC.	
E	12.00 BSC.	
E_1	10.00 BSC.	
L	0.45	0.75
N	64	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C64E-4R	4.7	5.0	5.3	4.7	5.0	5.3
C64E-9R	5.7	6.0	6.3	5.7	6.0	6.3

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 64L TQFP, 10x10x1.00mm EXPOSED PAD OPTION, INVERTED DIE PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0162	A	2/2